

36. (New) The system of claim 31, wherein the tester is a computer.
37. (New) A system comprising:
an integrated circuit (IC) including a plurality of pins; and
a tester connected to the IC to charge a selected pin among the plurality of pins to a known state at a first time and to sample a state of the selected pin at a second time different from the first time, wherein the tester is configured to determine a test result of the selected pin based on the state of the pin at the second time.
38. (New) The system of claim 37, wherein the tester is configured to apply a supply voltage to the selected pin at the first time.
39. (New) The system of claim 38, wherein the tester is configured to measure a voltage of the selected pin at the second time.
40. (New) The system of claim 39, wherein the IC is a Boundary Scan compliant IC.
41. (New) The system of claim 37, wherein the plurality of pins include a plurality of Boundary Scan pins, wherein the tester connects to the IC through the Boundary Scan pins.
42. (New) The system of claim 37, wherein the tester is a computer.
43. (New) A machine-readable medium having instructions stored thereon to cause a tester to perform a method, the method comprising:
driving a terminal on an integrated circuit (IC) to a state;
stopping the driving of the terminal;
floating the terminal for a predetermined time; and

RESPONSE TO RESTRICTION REQUIREMENT

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determining a state of the terminal after the predetermined time.

44. (New) The method of claim 43, wherein driving includes applying a logic low to the terminal.

45. (New) The method of claim 43, wherein driving includes applying a logic high to the terminal.

46. (New) The method of claim 43, wherein driving includes applying a voltage to the terminal.

47. (New) The method of claim 43, wherein determining includes measuring a voltage at the terminal after the predetermined time.

The Examiner is invited to contact Applicant's Representative at the below listed number if there are any questions regarding this Response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

TAWFIK R. ARABI ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
612-373-6969

Date 1-16-03

By

Viet V Tong
Reg. No. 45,416

CERTIFICATE UNDER 37 CFR 1.8 The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231 on this 16 day of January, 2003

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